A 2.4 GHz CMOS Ultra Low Power Low Noise Amplifier Design with 65 nm CMOS Technology

MinSuk Koo1, Hakchul Jung1, Ickhyun Song1, Hee-Sauk Jhon1, and Hyungcheol Shin1
1 School of Electrical Engineering and Computer Science, Seoul Nat’l Univ. Seoul, Korea
E-mail: korcom33@gmail.com

Abstract

In this paper, design approach of 2.4 GHz CMOS ultra low power Low Noise Amplifier (LNA) using 65 nm CMOS technology is presented. Conventional Inductively degenerated cascode topology where both MOS transistors are biased in sub-threshold region is used. There are many performance factors of LNAs such as signal power gain, noise factor, input referred 1-dB compression point (P1dB) and power consumption. In low power design, above all things proper power gain and low power consumption should be attained. This limitation makes ultra low power LNA optimization different from ordinary one. We analyze each performance factor in low power design and optimize figure of merit (FoM) with some specification goal.

1. Introduction

As the scaling-down of CMOS technology continues, the cut-off frequency, \( f_T \) and the maximum oscillation frequency, \( f_{MAX} \) of a MOS transistor has exceeded far more than several decades of gigahertz frequency, which extends the operation limit of CMOS circuits for wireless applications. Therefore, strong demand for ultra low power RFICs to extend the battery life of the wireless applications has arisen.

Traditionally, CMOS LNAs have been designed with MOS transistors operating in strong inversion regime rather than sub-threshold, MOSFETs do not have enough gain at sub-threshold region. However, with device scaling below 65nm, \( f_T \) and \( f_{MAX} \) are high enough at sub-threshold for RF IC design. (Fig. 1) Also, the minimum noise figure (NFmin) of deep sub-micron MOS transistors in sub-threshold regime remains constant [1]. Therefore, noise figure does not increase drastically as transistors goes to sub-threshold regime. Furthermore, drain current has an exponential dependence to the gate-source voltage in sub-threshold regime. As a result, transconductance to current ratio in sub-threshold region is larger than that in strong-inversion region.

Performance factors of LNAs such as signal power gain, input referred 1-dB compression point (P1dB) and power consumption are analyzed by measurement data and a 65 nm CMOS process design kit simulation. Since noise figure simulation is not accurate in sub-threshold region, calculation with analytics equation is performed for better accuracy. With this analysis, optimization for low power design is performed with over 10 dB of power gain and various power consumption specifications.

![Figure 1. \( f_T \) from H21](image)

2-1. Power gain and power consumption

Both MOS transistors used in cascade topology are biased in sub-threshold region for low power design of LNAs.

![Figure 2-(1). \( I_D \) and \( g_m \) vs. \( V_{gs} \) of cascade structure](image)
width needs the larger inductor for matching. And the larger inductor has the larger parasitic resistance of inductor. Therefore, optimization is needed in view of maximizing figure of merit (FoM).

2-2. Noise figure

Conventional cascade topology LNA schematic is shown in Fig. 5-(1). And small signal equivalent circuit with $C_{gd}$ consideration is shown in Fig. 5-(2).

As shown in Fig. 2-(1), (2), transconductance to current ratio in sub-threshold region is larger than that in strong-inversion region. And if we assume that width of $M_1$ and $M_2$ transistors are same, we can get gate-source voltage of $M_1$ transistor for specified power consumption for various width of device as shown in Fig. 3. Furthermore, we can obtain gain of each point as shown in Fig. 4 by using following gain equation. $f_{T1}$ and $f_{T2}$ are cut-off frequency of $M_1$ and $M_2$ transistors of cascade topology.

$$G = \frac{1}{4} \left[ \frac{f_{T1}}{f} \right]^2 \left( 1 + \left( \frac{f}{f_{T2}} \right)^2 \right)$$

(1)

Since too large inductor is needed for matching, the region with grey color in Fig. 4 cannot be used. The point using the smallest width of device for fixed power consumption can increased to the maximum gate-source voltage of $M_1$ transistor. And that point has largest gain for various power consumptions. However, the smaller
As scaling down the technology, the effect of the $C_{gd}$ is not ignored any more. From that equivalent circuit, the input matching condition and noise figure equation can be derived as below. [2] These conditions match well with design kit simulation.

$$
\begin{align*}
\text{Re}(Z_o) &= R_s \left( 1 + \frac{C_{gd}}{C_{gs}} \left( 1 + \frac{1}{R_m} \left( \frac{1}{C_{gs}} \left( 1 + \frac{1}{R_m} \right) \right) \right) \right) \\
\text{Im}(Z_o) &= \frac{R_s}{C_{gs}} \left( \frac{1}{R_m} \left( \frac{1}{C_{gs}} \left( 1 + \frac{1}{R_m} \right) \right) \right)
\end{align*}
$$

(2)

$$
NF - 1 = \frac{R_s}{R_{eq}} + \frac{4R_sN_f}{\eta} \left( \frac{1}{\eta} \right) \left( C_{gd} + C_m \left( 1 + \frac{R_m}{R_{eq}} \right) \right) \frac{2Q_{th}}{4kT}
$$

(3)

In sub-threshold region, $2qI_D$ is used for $S_{th}$. [3,4] The term related to channel thermal noise of $M_2$ is neglected because it is small at the operating frequency. [2] Dominant term of noise figure equation varies for frequency range. At low frequency, resistor source noise term $(R_s/R_{eq})$ is dominant. Whereas noise term related to transistor is dominant at high frequency. [5] At 2.4 GHz, resistor source noise term contributes over 90% of total value of NF-1. Therefore, we can simplify NF-1 as $R_s/R_{eq}$. Noise factor is shown in Fig. 6 as a function of width.

![Figure 6. Noise factor vs. width](image)

Since overall noise factor is dominated by resistor noise source term, parasitic resistor of gate inductor is important and the device with smaller width has larger noise figure.

2-3 Input referred 1-dB compression point ($P_{tdBin}$)

Input referred 1-dB compression point is shown in Fig. 7.

![Figure 7. $P_{tdBin}$ vs. $V_{gs}$](image)

As gate-source voltage increase, power gain increases for same power consumption. Therefore, $P_{tdBin}$ decreases. Since gain is larger at higher power consumption, $P_{tdBin}$ also decreases for higher power consumption.

2-4 FoM Optimization

The figure of merit is used to characterize the overall performance of the LNA circuit [6].

$$
\text{FoM} = \frac{Gain \cdot P_{tdBin} \cdot \text{frequency}}{(NF - 1) \cdot \text{Power}}
$$

(4)

Without $P_{tdBin}$ FoM is shown as Fig. 8-(1). Among them over 10 dB of power gain points are shown as Fig. 8-(2).

![Figure 8-(1). FoM without $P_{tdBin}$ vs. width without gain specification](image)
In this cases, the higher FoM was obtained with higher power consumption. However, $P_{dBm}$ decreases as power consumption increases. Total FoM is shown in Fig 9-(1), and over 10 dB power gain points are shown in Fig 9-(2).

FoM is maximized at 300 $\mu$W power consumption point. However, gain is smaller than 10 dB at this condition.

Optimum FoM design which satisfies power gain of above 1 dB, is obtained. Power consumption is 400 $\mu$W with optimum bias of $V_{gs} = 0.376$ V. Width of device is about 100 $\mu$m. FoM is optimized at 6.5.

3. Conclusion

In this paper, we optimized FoM with power gain and power consumption specifications. In low power design, these specifications should be satisfied. Furthermore, $P_{dBm}$ should be considered. We analyze each performance factor in low power design and optimize figure of merit (FoM) with some specification goal. FoM of 6.5 was obtained at $V_{gs}=0.38$ V with power consumption of 400 $\mu$W and device width of 100 $\mu$m.

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References